Ratiometric Linear Hall Effect Sensor ICs for High-Temperature Operation

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: October 31, 2011

- for the A1321EUA-T and the A1321LUA-T use the *A1324LUA-T*
- for the A1321ELHLT-T and the A1321LLHLT-T use the *A1324LLHLX-T*
- for the A1322LUA-T use the *A1325LUA-T*
- for the A1322LLHLT-T use the *A1325LLHLX-T*
- for the A1323EUA-T and the A1323LUA-T use the *A1326LUA-T*
- for the A1323LLHLT-T use the *A1326LLHLX-T*

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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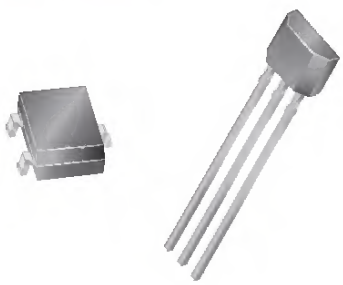
A1321, A1322, and A1323

Ratiometric Linear Hall Effect Sensor ICs for High-Temperature Operation

Features and Benefits

- Temperature-stable quiescent output voltage
- Precise recoverability after temperature cycling
- Output voltage proportional to magnetic flux density
- Ratiometric rail-to-rail output
- Improved sensitivity
- 4.5 to 5.5 V operation
- Immunity to mechanical stress
- Solid-state reliability
- Robust EMC protection

Packages: 3 pin SOT23W (suffix LH), and 3 pin SIP (suffix UA)



Not to scale

Description

The A132X family of linear Hall-effect sensor ICs are optimized, sensitive, and temperature-stable. These ratiometric Hall-effect sensor ICs provide a voltage output that is proportional to the applied magnetic field. The A132X family has a quiescent output voltage that is 50% of the supply voltage and output sensitivity options of 2.5 mV/G, 3.125 mV/G, and 5m V/G. The features of this family of devices are ideal for use in the harsh environments found in automotive and industrial linear and rotary position sensing systems.

Each device has a BiCMOS monolithic circuit which integrates a Hall element, improved temperature-compensating circuitry to reduce the intrinsic sensitivity drift of the Hall element, a small-signal high-gain amplifier, and a rail-to-rail low-impedance output stage.

A proprietary dynamic offset cancellation technique, with an internal high-frequency clock, reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress. The high frequency clock allows for a greater sampling rate, which results in higher accuracy and faster signal processing capability. This technique produces devices that have an extremely stable quiescent output voltage, are immune to mechanical stress, and have precise

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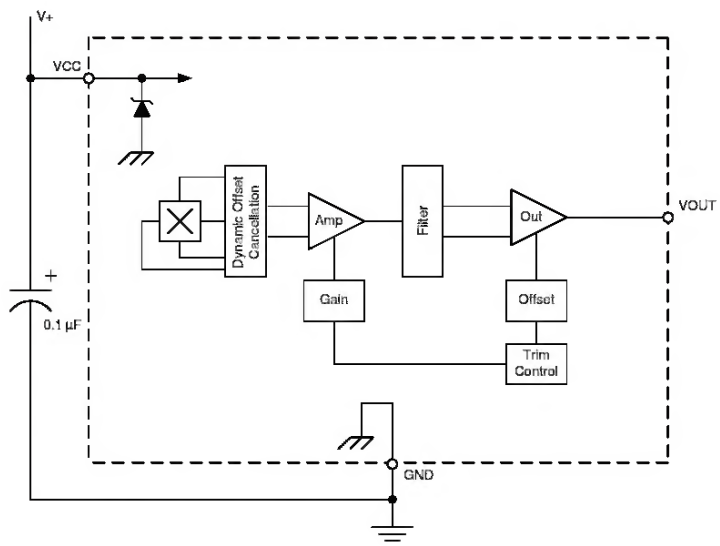
Functional Block Diagram



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Description (continued)

recoverability after temperature cycling. Having the Hall element and an amplifier on a single chip minimizes many problems normally associated with low-level analog signals.

Output precision is obtained by internal gain and offset trim adjustments made at end-of-line during the manufacturing process.

The A132X family is provided in a 3-pin single in-line package (UA) and a 3-pin surface mount package (LH). Each package is available in a lead (Pb) free version (suffix, –T) , with a 100% matte tin plated leadframe.

Selection Guide

Part Number	Packing[1]	Mounting	Ambient, T_A (ºC)	Sensitivity, Typ. (mV/G)
~~A1321ELHLT-T~~[2]	7-in. reel, 3000 pieces/reel	Surface Mount	–40 to 85	5.000
~~A1321EUA-T~~[3]	Bulk, 500 pieces/bag	SIP through hole		
~~A1321LLHLT-T~~[2]	7-in. reel, 3000 pieces/reel	Surface Mount	–40 to 150	
~~A1321LUA-T~~[3]	Bulk, 500 pieces/bag	SIP through hole		
~~A1322LLHLT-T~~[2]	7-in. reel, 3000 pieces/reel	Surface Mount	–40 to 150	3.125
~~A1322LUA-T~~[3]	Bulk, 500 pieces/bag	SIP through hole		
~~A1323EUA-T~~[3]	Bulk, 500 pieces/bag	SIP through hole	–40 to 85	2.500
~~A1323LLHLT-T~~[2]	7-in. reel, 3000 pieces/reel	Surface Mount	–40 to 150	
~~A1323LUA-T~~[3]	Bulk, 500 pieces/bag	SIP through hole		

[1]Contact Allegro for additional packing options.
[2]This variant is in production, however, it has been deemed Pre-End of Life. The product is approaching end of life. Within a minimum of 6 months, the device will enter its final, Last Time Buy, order phase. Status change: January 31, 2011. Suggested replacements: for the A1321ELHLT-T and the A1321LLHLT-T use the A1324LLHLX-T, for the A1322LLHLT-T use the A1325LLHLX-T, and for the A1323LLHLT-T use the A1326LLHLX-T.
[3]Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: January 31, 2011.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}	*Additional current draw may be observed at voltages above the minimum supply Zener clamp voltage, $V_{Z(min)}$, due to the Zener diode turning on.	8	V
Output Voltage	V_{OUT}		8	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Output Sink Current	I_{OUT}		10	mA
Operating Ambient Temperature	T_A	Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

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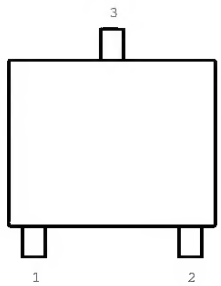
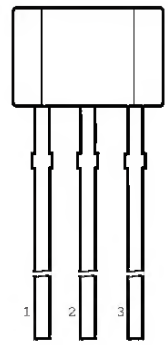
Pin-out Drawings

Package LH



Package UA



Terminal List

Symbol	Number		Description
	Package LH	Package UA	
VCC	1	1	Connects power supply to chip
VOUT	2	3	Output from circuit
GND	3	2	Ground

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DEVICE CHARACTERISTICS[1] over operating temperature (T_A) range, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Units
Electrical Characteristics; V_{CC} = 5 V, unless otherwise noted						
Supply Voltage	$V_{cc(op)}$	Operating; Tj < 165°C	4.5	5.0	5.5	V
Supply Current	I_{cc}	B = 0, I_{out} = 0	–	5.6	8	mA
Quiescent Voltage	$V_{out(q)}$	B = 0, T_A = 25°C, I_{out} = 1 mA	2.425	2.5	2.575	V
Output Voltage[3]	$V_{out(H)}$	B = +**X**, I_{out} = –1 mA	–	4.7	–	V
	$V_{out(L)}$	B = –**X**, I_{out} = 1 mA	–	0.2	–	V
Output Source Current Limit[3]	$I_{out(LM)}$	B = –**X**, $V_{out} \rightarrow 0$	–1.0	–1.5	–	mA
Supply Zener Clamp Voltage	V_Z	I_{CC} = 11 mA = $I_{cc(max)}$ + 3	6	8.3	–	V
Output Bandwidth	BW		–	30	–	kHz
Clock Frequency	f_C		–	150	–	kHz
Output Characteristics; over V_{CC} range, unless otherwise noted						
Noise, Peak-to-Peak[4]	V_N	A1321; C_{bypass} = 0.1 µF, no load	–	–	40	mV
		A1322; C_{bypass} = 0.1 µF, no load	–	–	25	mV
		A1323; C_{bypass} = 0.1 µF, no load	–	–	20	mV
Output Resistance	R_{out}	$I_{out} \leq \pm 1$ mA	–	1.5	3	Ω
Output Load Resistance	R_L	$I_{out} \leq \pm 1$ mA, VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance	C_L	VOUT to GND	–	–	10	nF

[1] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.

[2] Typical data is at T_A = 25°C. They are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

[3] In these tests, the vector **X** is intended to represent positive and negative fields sufficient to swing the output driver between fully OFF and saturated (ON), respectively. It is NOT intended to indicate a range of linear operation.

[4] Noise specification includes both digital and analog noise.

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MAGNETIC CHARACTERISTICS[1,2] over operating temperature range, T_A; V_{CC} = 5 V, I_{out} = –1 mA; unless otherwise noted

Characteristics	Symbol	Test Condition	Min	Typ[3]	Max	Units[4]
Sensitivity[5]	Sens	A1321; T_A = 25°C	4.750	5.000	5.250	mV/G
		A1322; T_A = 25°C	2.969	3.125	3.281	mV/G
		A1323; T_A = 25°C	2.375	2.500	2.625	mV/G
Delta $V_{out(q)}$ as a function of temperature	$V_{out(q)(\Delta T)}$	Defined in terms of magnetic flux density, B	–	–	±10	G
Ratiometry, $V_{out(q)}$	$V_{out(q)(\Delta V)}$		–	–	±1.5	%
Ratiometry, Sens	$\Delta Sens_{(\Delta V)}$		–	–	±1.5	%
Positive Linearity	Lin+		–	–	±1.5	%
Negative Linearity	Lin–		–	–	±1.5	%
Symmetry	Sym		–	–	±1.5	%
UA Package						
Delta Sens at T_A = max[5]	$\Delta Sens_{(TAmax)}$	From hot to room temperature	–2.5	–	7.5	%
Delta Sens at T_A = min[5]	$\Delta Sens_{(TAmin)}$	From cold to room temperature	–6	–	4	%
Sensitivity Drift[6]	$Sens_{Drift}$	T_A = 25°C; after temperature cycling and over time	–	±2	–	%
LH Package						
Delta Sens at T_A = max[5]	$\Delta Sens_{(TAmax)}$	From hot to room temperature	–5	–	5	%
Delta Sens at T_A = min[5]	$\Delta Sens_{(TAmin)}$	From cold to room temperature	–3.5	–	8.5	%
Sensitivity Drift[6]	$Sens_{Drift}$	T_A = 25°C; after temperature cycling and over time	–	±2	–	%

[1] Additional information on characteristics is provided in the section Characteristics Definitions, on the next page.
[2] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
[3] Typical data is at T_A = 25°C, except for ΔSens, and at *x.x* Sens. Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits. In addition, the typical values vary with gain.
[4] 10 G = 1 millitesla.
[5] After 150°C pre-bake and factory programming.
[6] Sensitivity drift is the amount of recovery with time.

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Characteristic Definitions

Quiescent Voltage Output. In the quiescent state (no magnetic field), the output equals one half of the supply voltage over the operating voltage range and the operating temperature range. Due to internal component tolerances and thermal considerations, there is a tolerance on the quiescent voltage output both as a function of supply voltage and as a function of ambient temperature. For purposes of specification, the quiescent voltage output as a function of temperature is defined in terms of magnetic flux density, B, as:

$$\Delta V_{out(q)(\Delta T)} = \frac{V_{out(q)(T_A)} - V_{out(q)(25°C)}}{Sens_{(25°C)}} \quad (1)$$

This calculation yields the device's equivalent accuracy, over the operating temperature range, in gauss (G).

Sensitivity. The presence of a south-pole magnetic field perpendicular to the package face (the branded surface) increases the output voltage from its quiescent value toward the supply voltage rail by an amount proportional to the magnetic field applied. Conversely, the application of a north pole will decrease the output voltage from its quiescent value. This proportionality is specified as the sensitivity of the device and is defined as:

$$Sens = \frac{V_{out(-B)} - V_{out(+B)}}{2B} \quad (2)$$

The stability of sensitivity as a function of temperature is defined as:

$$\Delta Sens_{(\Delta T)} = \frac{Sens_{(T_A)} - Sens_{(25°C)}}{Sens_{(25°C)}} \times 100\% \quad (3)$$

Ratiometric. The A132X family features a ratiometric output. The quiescent voltage output and sensitivity are proportional to the supply voltage (ratiometric).

The percent ratiometric change in the quiescent voltage output is defined as:

$$\Delta V_{out(q)(\Delta V)} = \frac{V_{out(q)(V_{CC})} / V_{out(q)(5V)}}{V_{CC} / 5\ V} \times 100\% \quad (4)$$

and the percent ratiometric change in sensitivity is defined as:

$$\Delta Sens_{(\Delta V)} = \frac{Sens_{(V_{CC})} / Sens_{(5V)}}{V_{CC} / 5\ V} \times 100\% \quad (5)$$

Linearity and Symmetry. The on-chip output stage is designed to provide a linear output with a supply voltage of 5 V. Although application of very high magnetic fields will not damage these devices, it will force the output into a non-linear region. Linearity in percent is measured and defined as:

$$Lin+ = \frac{V_{out(+B)} - V_{out(q)}}{2(V_{out(+B/2)} - V_{out(q)})} \times 100\% \quad (6)$$

$$Lin- = \frac{V_{out(-B)} - V_{out(q)}}{2(V_{out(-B/2)} - V_{out(q)})} \times 100\% \quad (7)$$

and output symmetry as:

$$Sym = \frac{V_{out(+B)} - V_{out(q)}}{V_{out(q)} - V_{out(-B)}} \times 100\% \quad (8)$$

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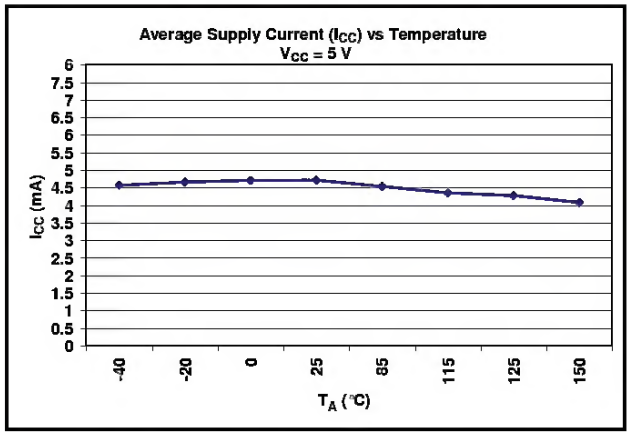
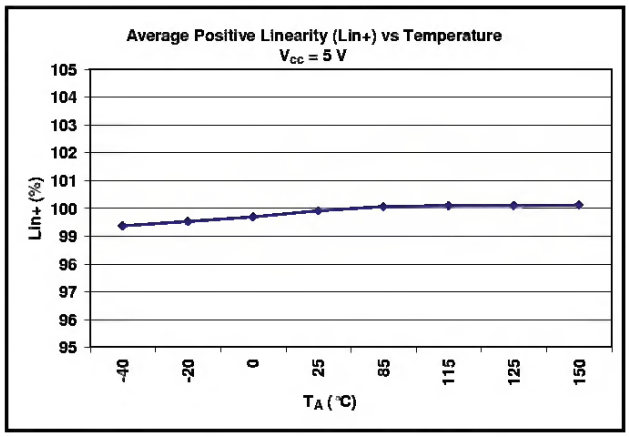
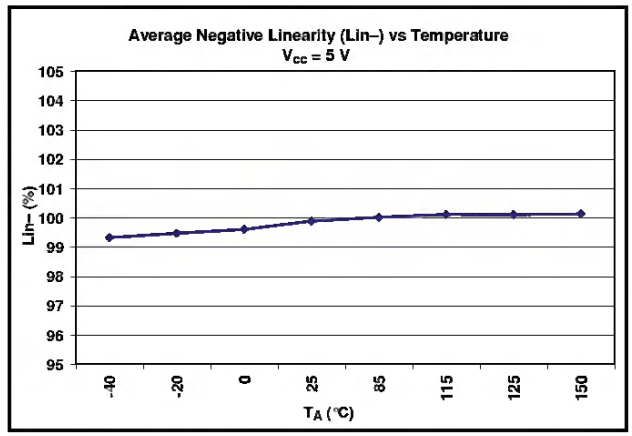
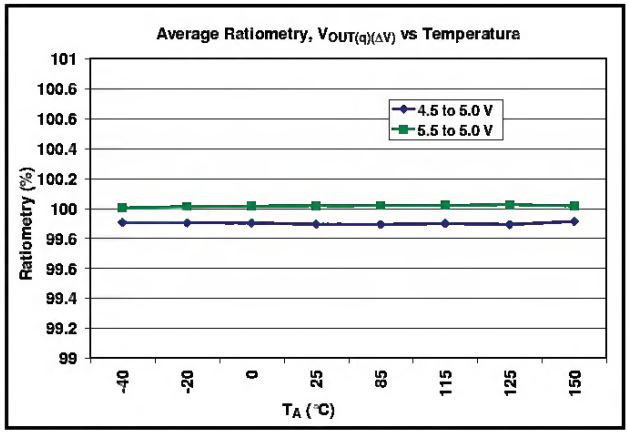
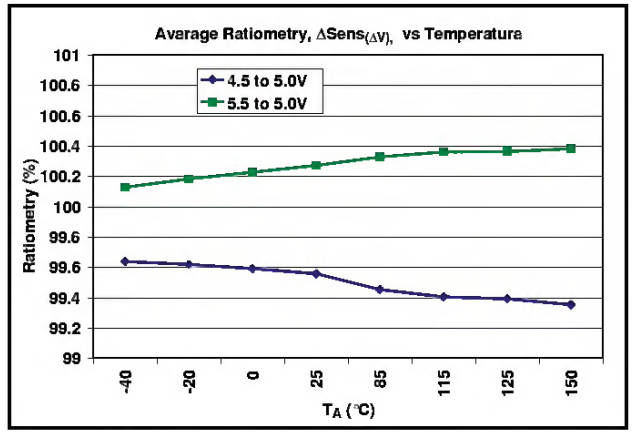
Typical Characteristics
(30 pieces, 3 fabrication lots)











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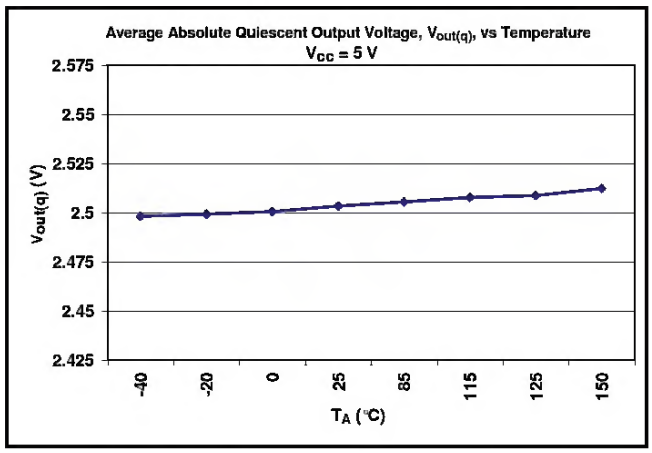
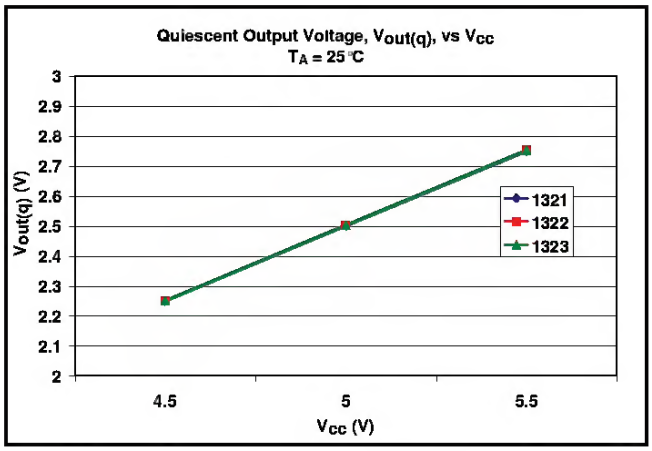
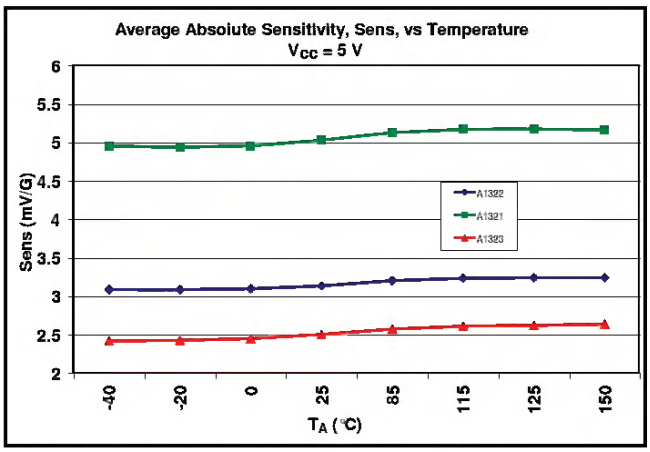
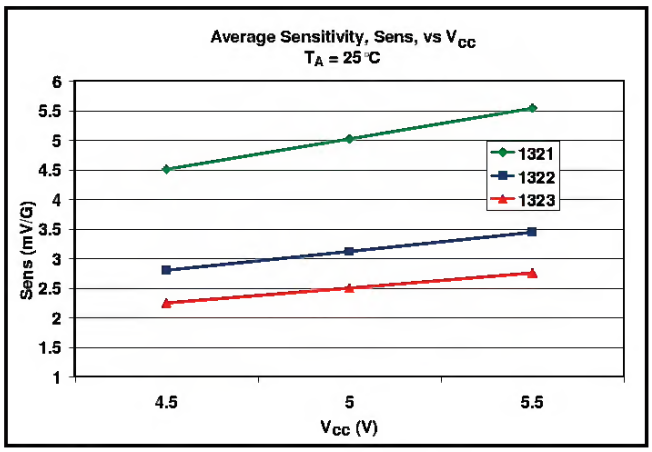
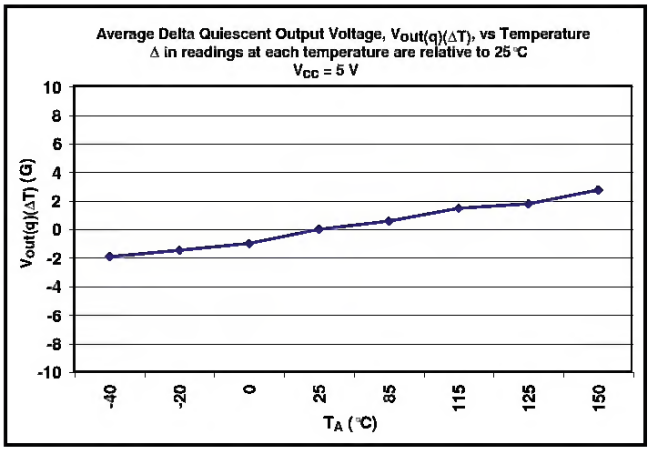
Typical Characteristics, continued
(30 pieces, 3 fabrication lots)

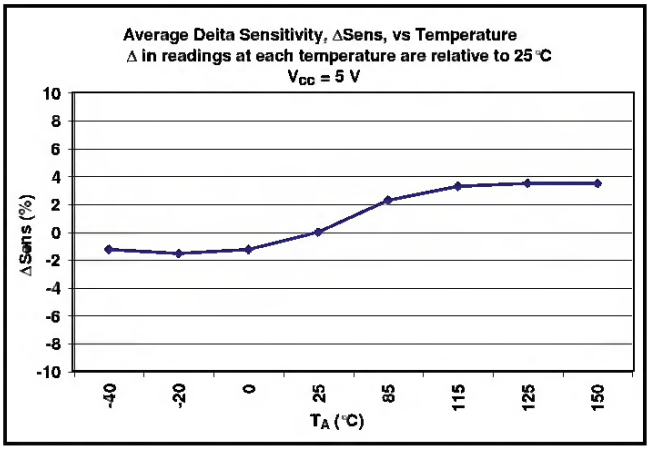












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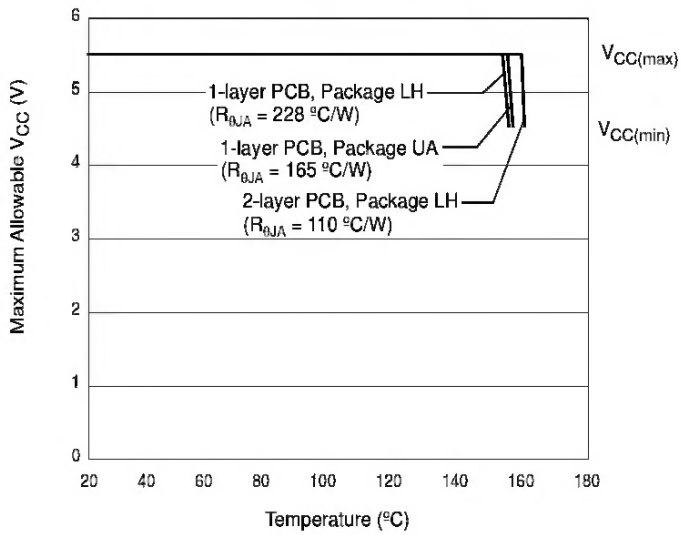
THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

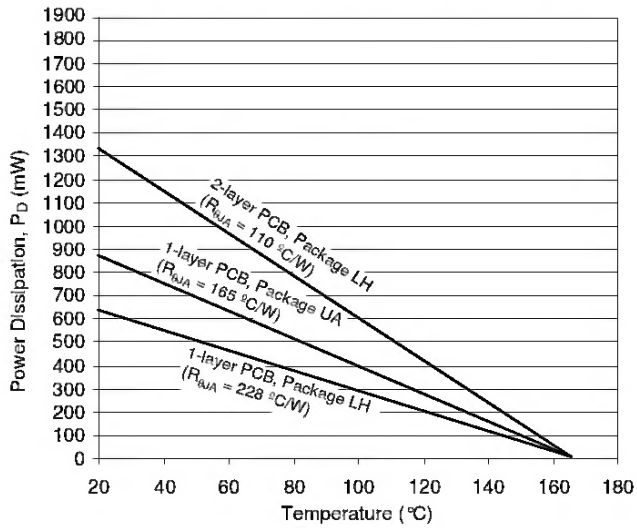
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W

*Additional thermal information available on Allegro website.

Power Derating Curve



Power Dissipation versus Ambient Temperature



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Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: $T_A = 25°C$, $V_{CC} = 12$ V, $I_{CC} = 4$ mA, and $R_{\theta JA} = 140$ °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12 \text{ V} \times 4 \text{ mA} = 48 \text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 48 \text{ mW} \times 140 \text{ °C/W} = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at $T_A = 150°C$, package UA, using minimum-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA} = 165°C/W$, $T_{J(max)} = 165°C$, $V_{CC(max)} = 5.5$ V, and $I_{CC(max)} = 8$ mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165 \text{ °C/W} = 91 \text{ mW}$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 91 \text{ mW} \div 8 \text{ mA} = 11.4 \text{ V}$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

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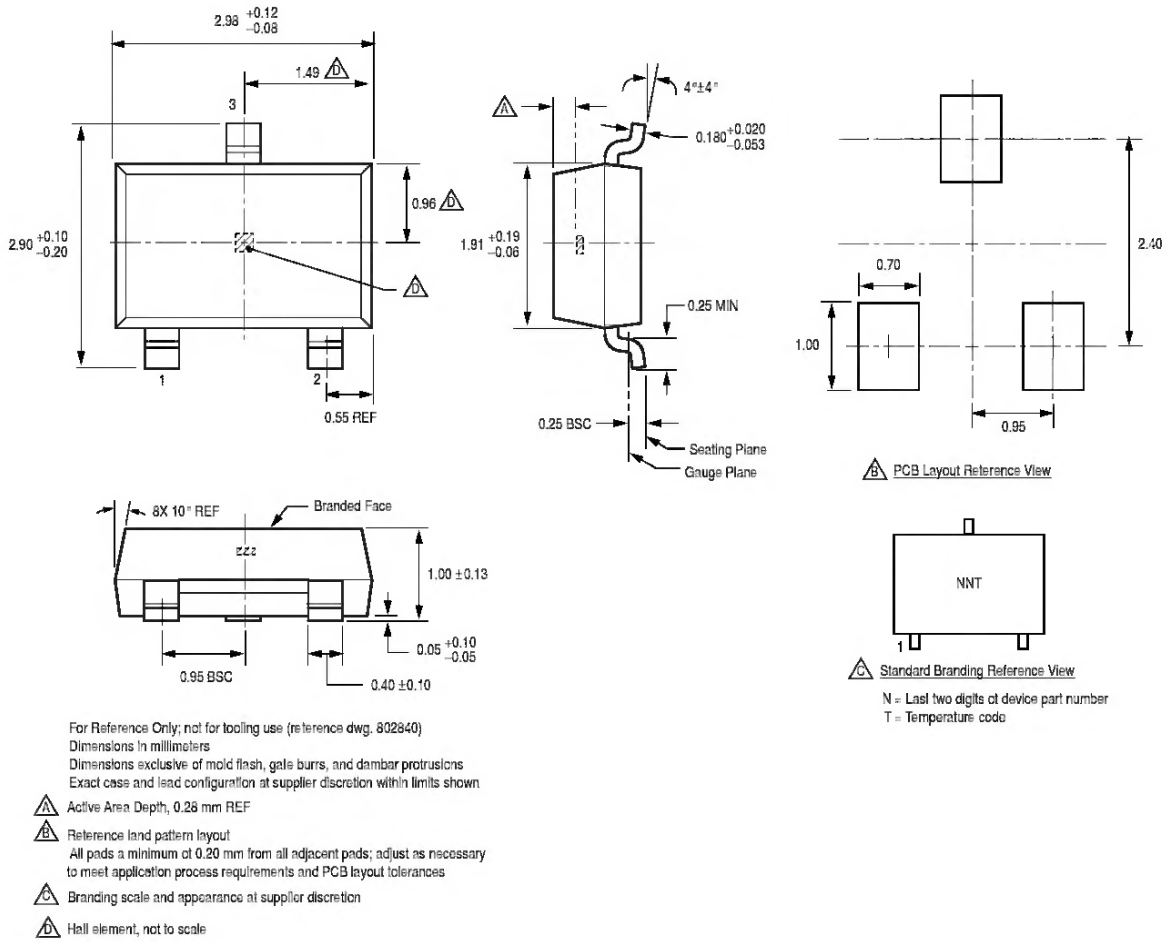
Package LH, 3-Pin (SOT-23W)



For Reference Only; not for tooling use (reference dwg. 802840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Active Area Depth, 0.28 mm REF

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

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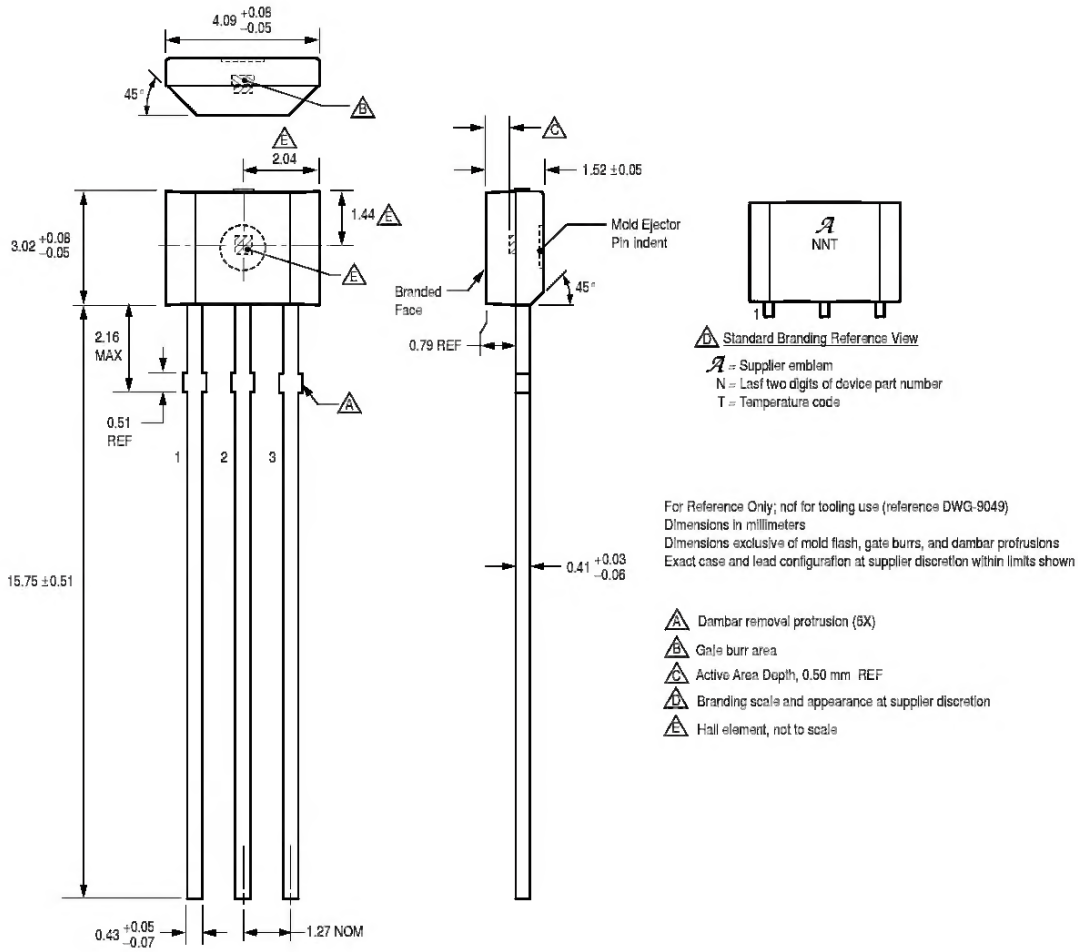
Package UA, 3-Pin SIP



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Allegro MicroSystems, Inc.
115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
1.508.853.5000; www.allegromicro.com

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